

ABSTRACT:

ESD Design-for-Reliability: A STRESS Challenge for ICs

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Electrostatic discharge (ESD) remains a major reliability problem to integrated circuits (ICs), particularly at advanced technology nodes and for emerging hetero-integrated systems-on-integrated-chiplets (SoICs). This talk will discuss fundamentals of ESD failures, advances in on-chip ESD protection, practical ESD protection designs for ICs, and future directions for ESD protection research. Recent advances in 3D effects of ESD stressing on ESD protection designs in advance CMOS technologies will be presented.